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Ferroelectric Polarization Switching of Hafnium Zirconium Oxide in

a Ferroelectric/Dielectric Stack

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| Downloaded via UNIV OF SOUTHERN INDIANA on July 23, 2019 at 01:58:12 (UTC).  See https://pubs.acs.org/sharingguidelines for options on how to legitimately share published articles. | ABSTRACT: The ferroelectric polarization switching in ferroelectric hafnium | | | | |  |  |  |  |  |
| zirconium oxide (Hf0.5Zr0.5O2, HZO) in the HZO/Al2O3 ferroelectric/dielectric stack is investigated systematically by capacitance−voltage and polarization− | | | | |
| voltage measurements. The thickness of dielectric layer is found to have a | | | | |
| determinant impact on the ferroelectric polarization switching of ferroelectric | | | | |
| HZO. A suppression of ferroelectricity is observed with a thick dielectric layer. In | | | | |
| the gate stacks with thin dielectric layers, a full polarization switching of the | | | | |
| ferroelectric layer is found possible by the proposed leakage-current-assist | | | | |
| mechanism through the ultrathin dielectric layer. Theoretical simulation results agree well with experimental data. This work clarifies some of the critical parts of the long-standing confusions and debate related to negative capacitance field-effect | | | | |
| transistors (NC-FETs) concepts and experiments. | | | | |
| KEYWORDS: ferroelectric, HZO, Fe-FET, negative capacitance, steep-slope | | | | | | | | | |
| ■INTRODUCTION  A ferroelectric material has two stable polarization states with different directions, which are switchable by the external electric field, and thus is extensively explored for nonvolatile memory applications. Using ferroelectric field-effect transistors (Fe-  FETs) as FET-type ferroelectric memory is a promising  ferroelectric memory architecture because of its high density and nondestructive readout.1−4Recently, using a ferroelectric-gated transistor as a negative capacitance field-effect transistor  (NC-FET) has attracted tremendous attention as a novel steep-slope device.5−9In both Fe-FET and NC-FET, a ferroelectric  (FE) insulator and linear dielectric (DE) insulator bilayer stack10−17is applied as the gate structure. The necessity of such a  linear DE layer is because an interfacial oxide layer between the  semiconductor channel and FE insulator is required to improve  the ferroelectric/semiconductor interface and meanwhile provide sufficient capacitance matching if the quasi-static  negative capacitance (QSNC) concept is applied for the development of NC-FETs.5The QSNC definition was introduced to distinguish between the stabilized NC effect and transient NC effect.18One important fact, which has been  overlooked in the past several years, is that the FE/DE stack capacitor is fundamentally different from an FE capacitor and DE capacitor in series.18,19Therefore, the complete under-  standing of the impact of the DE layer on the ferroelectric  properties of an FE/DE stack is crucial to study of the  ferroelectric switching mechanism in Fe-FETs and NC-FETs. | | this study, and Al2O3 is chosen as the linear DE insulator to study the ferroelectric polarization switching in the FE/DE stack. It is well-known that ferroelectric HZO has a thickness-dependent remnant polarization (Pr) at about 10−30 μC/cm.2,22,23 However, a conventional dielectric insulator cannot support such a large charge density. For example, Al2O3 has a typical dielectric constant of 8 and a breakdown electric field less than 1 V/nm.24The calculated charge density at breakdown electric field is about 7 μC/cm2, which is the maximum charge density (Qmax) for ideal Al2O3 to be able to support without breakdown. Note that in reality, this value for Qmax is much smaller. As can be seen, even in ideal case, there is a big gap between the remnant polarization in HZO and the maximum charge density in Al2O3. This fact can also be generally applied to other FE/DE stack systems. Thus, the puzzle and confusion in the field is how can ferroelectric polarization switching happen in an FE/DE stack without sufficient charge balance? Such charge difference can only be explained by introducing the leakage-current and interfacial charges. The impact of leakage current in FE/DE bilayer was previously reported, and the interfacial charging is believed to be important in the ferroelectric switching process by a thermodynamic free energy model.10In FE hafnium oxide systems, the discussions are mostly focused on the impact of leakage current on the negative capacitance effect.15−17,25The hysteresis-free NC effect in HZO/Al2O3 is reported by fast pulse measurement; the impacts of leakage current and charge trapping are minimized because of the fast pulses.15−17,26 | | | | | | | |
| Ferroelectric hafnium oxide, such as hafnium zirconium oxide | | | | | | | | | |
| (Hf0.5Zr0.5O2, HZO), has been recently discovered as an | | Received: | February 13, 2019 | | | | | | |
| ultrathin CMOS compatible high performance ferroelectric insulator.20,21Therefore, HZO is chosen as the FE insulator for | | Accepted: | | May 8, 2019 | | | | | |
| Published: May 8, 2019 | | | | | | | |
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In this work, we provide a simple understanding of the ferroelectric polarization switching process in an FE/DE stack by introducing the leakage current through the thin DE layer and only considering the electrostatics. The ferroelectric polarization switching of HZO in the HZO/Al2O3 FE/DE stack is investigated systematically by capacitance−voltage (C−V) and polarization−voltage (P−V) measurements. The thickness of the dielectric layer is found to have determinant impact on the ferroelectric polarization switching of ferroelectric HZO. The suppression of ferroelectricity is observed with thick dielectric layer. In the gate stacks with thin dielectric layers, a full polarization switching of the ferroelectric layer is found possible by the proposed leakage-current-assist mechanism through the ultrathin dielectric layer. It is confirmed that the charge needed for ferroelectric polarization switching comes from the leakage current through the thin dielectric layer. Without such leakage current to realize the charge balance, the FE HZO cannot be fully polarized.

■EXPERIMENTAL SECTION   
Figure 1 shows the experimental device structures. Four types of capacitor structures are used in this work: (a) TiN/Al2O3/TiN (type

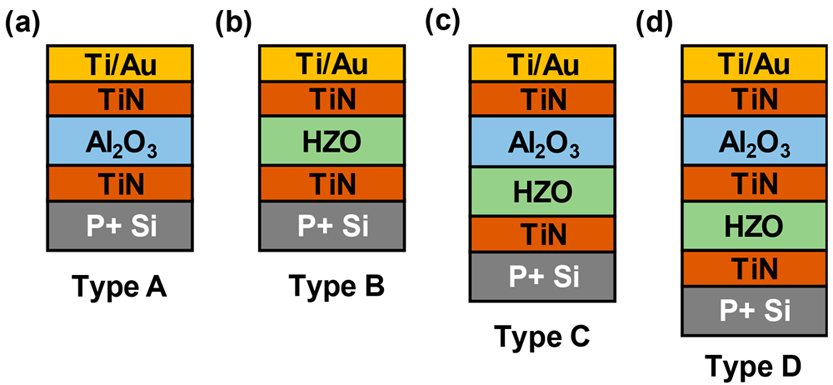


Figure 1. Capacitor structures used in this work. (a) Al2O3 only (type A), (b) HZO only (type B), (c) Al2O3 and HZO stack without internal metal (type C), and (d) Al2O3 and HZO stack with TiN layer as the internal metal (type D).

A), (b) TiN/HZO/TiN (type B), (c) TiN/Al2O3/HZO/TiN (type C), and (d) TiN/Al2O3/TiN/HZO/TiN (type D). The device fabrication process started with the standard solvent cleaning of heavily p-doped Si substrates (resistivity < 0.005 Ω·cm). TiN was deposited by atomic layer deposition (ALD) at 250 °C, using [(CH3)2N]4Ti (TDMAT, heated up to 60 °C) and NH3 as the Ti and N precursors, respectively. All TiN layers are metallic and 30 nm thick. Hf1−xZrxO2 film was deposited by ALD at 200 °C, using [(CH3)2N]4Hf (TDMAHf, heated up to 60 °C), [(CH3)2N]4Zr (TDMAZr, heated up to 75 °C), and H2O as the Hf, Zr, and O precursors, respectively. The Hf1−xZrxO2

film with x = 0.5 was achieved by controlling the HfO2/ZrO2 cycle ratio of 1:1. The ALD deposition of TiN and HZO was in two separated ALD

chambers to avoid cross-contamination. The two ALD chambers are

connected externally by an Ar environment in a glovebox to avoid environmental contamination. After the deposition of type A−D structures, the samples were annealed at 500 °C in N2 environment for 1 min by rapid thermal annealing. Then, Ti/Au top electrodes were fabricated by photolithography, e-beam evaporation, and a lift-off process (capacitor area = 5024 μm2). CF4/Ar dry etching was done to remove top TiN layer for device isolation for type A−C capacitors. For

type D capacitors, BCl3/Ar dry etching was used to remove the top Al2O3 layer, and CF4/Ar dry etching was used to remove the top and middle TiN layers. All electrical measurements were done at room temperature in a cascade summit probe station. C−V measurement was performed using an Agilent E4980A LCR meter, and P−V measure-

ment was carried out using a Radiant RT66C ferroelectric tester.

■RESULTS AND DISCUSSION   
Figure 2(a) shows the C−V measurement of a type A capacitor

with 20 nm Al2O3, from 1 kHz to 1 MHz. Figure 2(b) shows the P−V measurement of the same type A capacitor, showing a

linear dielectric characteristic. Both measurements (small signal C−V, dP/dV in P−V) give consistent capacitance values for the type A dielectric capacitor with a capacitance of ∼0.33 μF/cm2 and a corresponding dielectric constant of ∼8. Figure 3(a) shows the C−V measurement of a type B capacitor with 20 nm HZO, from 1 kHz to 1 MHz. The C−V measurement of a type B capacitor shows two signature peaks in the C−V hysteresis loop as the ferroelectric characteristics. The different capacitances at different voltages in C−V are attributed to the different dielectric constant due to the difference in atomic structures in different

ferroelectric polarization states. The corresponding dielectric

constants are calculated, as also shown in the right axis. Figure 3(b) shows the P−V measurement of the same type B capacitor,

showing a ferroelectric hysteresis loop.

Figure 4(a) shows the C−V measurements of type C

capacitors with 20 nm HZO and Al2O3 from 0 to 20 nm, measured at 10 kHz. The capacitances of type C capacitors

decrease with thicker Al2O3 as expected. The signature two capacitance peaks due to ferroelectricity in the C−V hysteresis

loop decrease and eventually disappear in the 20 nm HZO/20

nm Al2O3 stack, suggesting the reduction of ferroelectricity in the thick DE layer and FE layer stack. This feature is even more clearly presented in Figure 4(b), which shows the P−V

measurements of type C capacitors with 20 nm HZO and

Al2O3 from 4 to 20 nm. The applied voltage ranges are maximized in P−V measurement before the leakage current has essential impacts. The significant decrease of remnant polar-

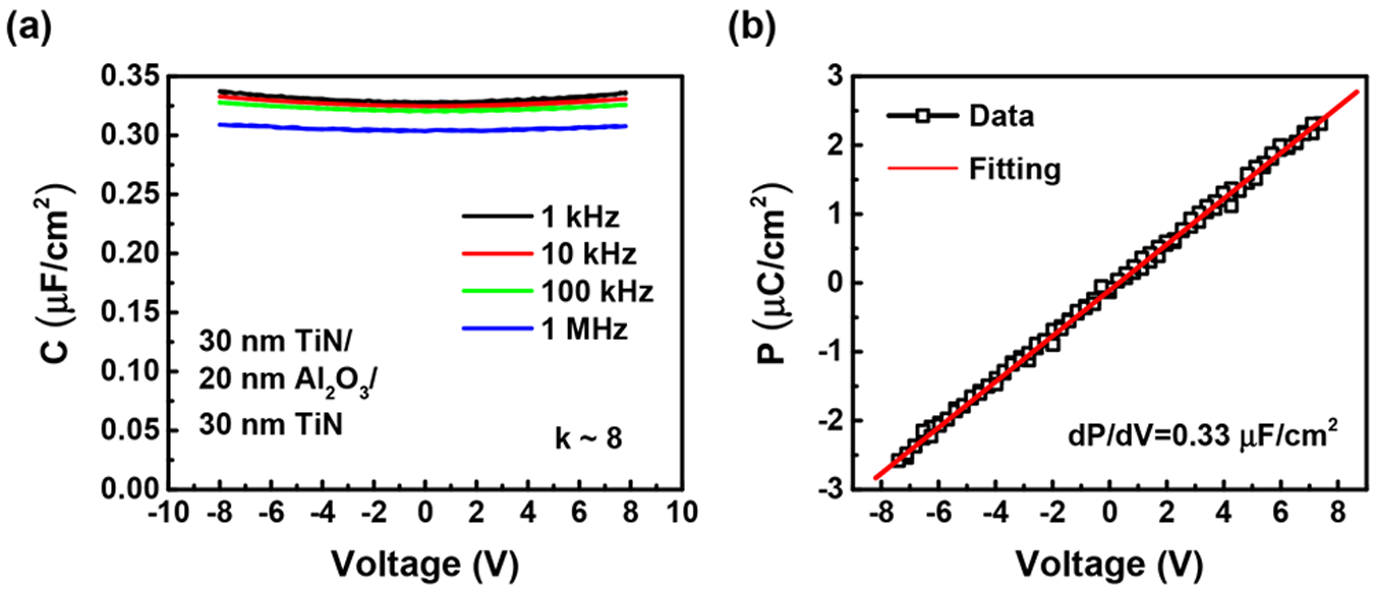


Figure 2. (a) C−V measurement and (b) P−V measurement on a type A capacitor with 20 nm Al2O3.

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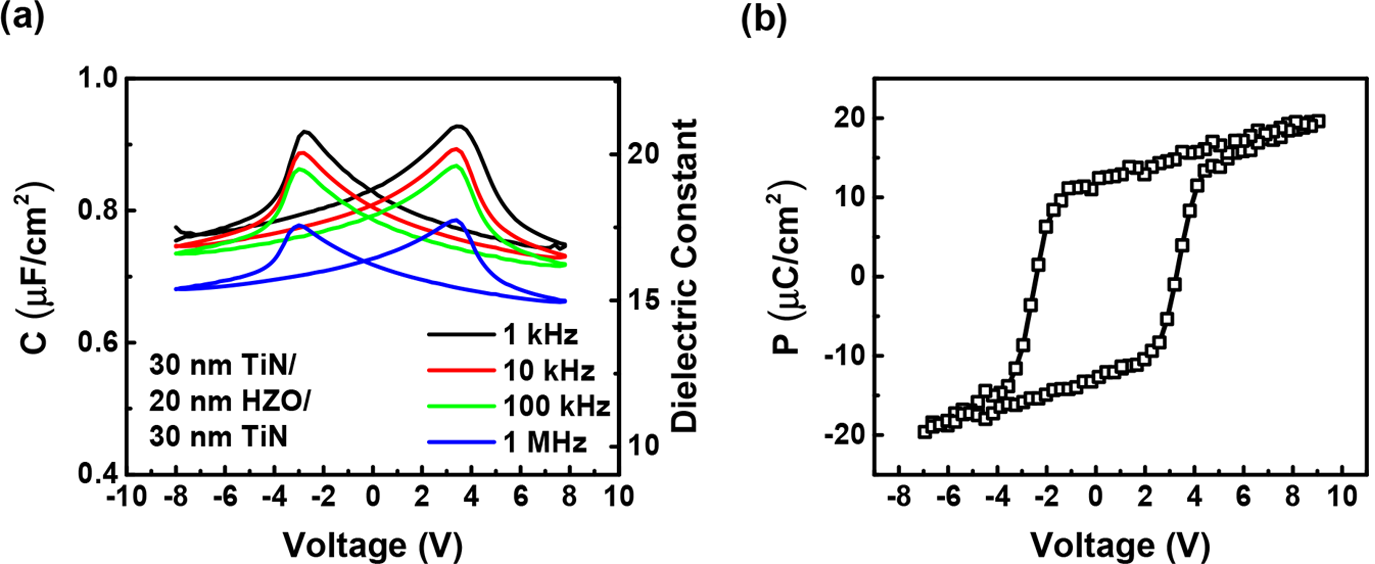


Figure 3. (a) C−V measurement and (b) P−V measurement of a type B capacitor with 20 nm HZO.

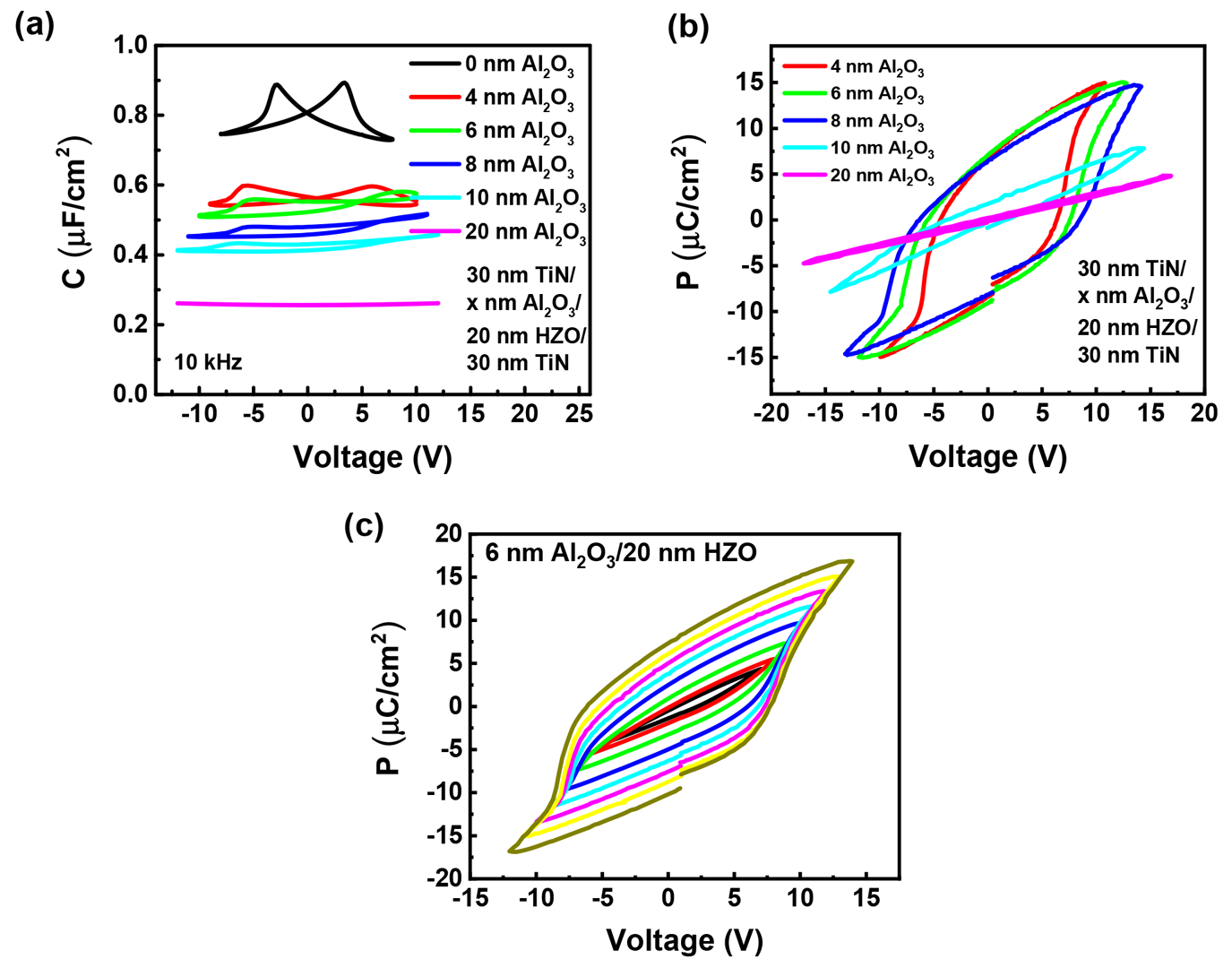


Figure 4. (a) C−V measurements and (b) P−V measurements on type C capacitors with different Al2O3 thicknesses and 20 nm HZO. (c) P−V measurements on a type C capacitor with 6 nm Al2O3 and 20 nm HZO at different voltage sweep ranges.

ization in P−V hysteresis loops is clearly observed with thicker DE layers. The C−V measurements and P−V measurements consistently confirm that a thick DE layer can suppress the ferroelectricity in the FE/DE stack. Figure 4(c) shows the P−V characteristics of an FE/DE capacitor with 20 nm HZO and 6 nm Al2O3, measured at different voltage sweep ranges. The coercive voltage and remnant polarization are found to be dependent on the sweep voltage range.

To further understand the physics behind the DE layer thickness dependence on the ferroelectricity of the FE/DE stack, a theoretical analysis is provided, as shown in Figure 5. To understand the dynamic process of ferroelectric switching, this process is plotted by a two-step process: before ferroelectric polarization switching and after ferroelectric polarization switching. As is well-known, the ferroelectric polarization switching is atom reposition within the unit cell, so it is always slower than the electron redistribution. Thus, the two-step assumption is valid. For simplicity, it is assumed the FE layer has a dielectric constant of ϵFE (without considering ferroelectric polarization) and a thickness of tFE; the DE layer has a dielectric constant of ϵDE and a thickness of tDE. It also assumes that the FE

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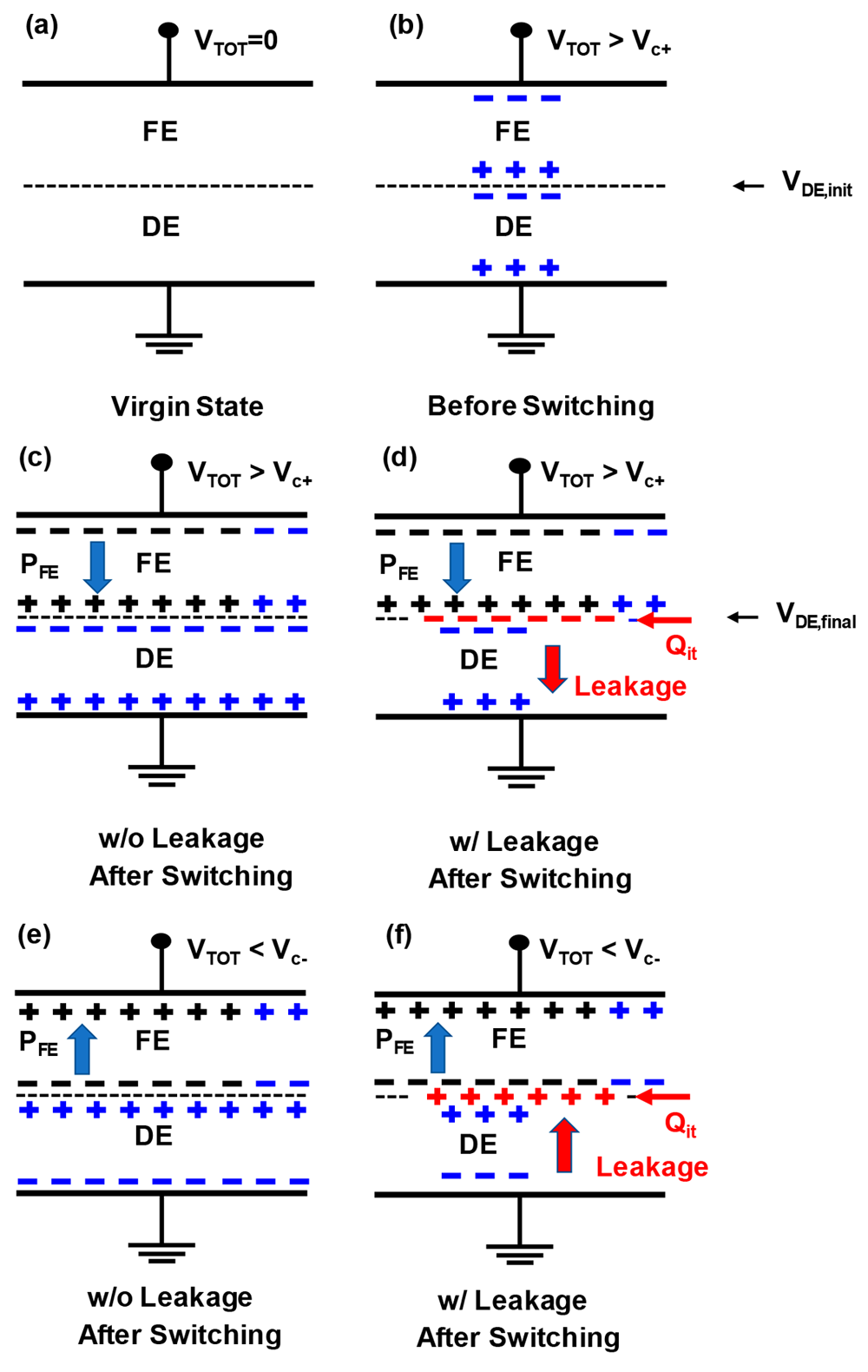


Figure 5. Illustration of charge distribution in FE/DE stack in the

following conditions. (a) VTOT = 0, and FE layer is not polarized. (b) VTOT larger than positive coercive voltage Vc+ before polarization switching. VTOT larger than positive coercive voltage Vc+ after polarization switching (c) assuming no leakage current through the

DE layer and (d) assuming the existence of leakage current through the

DE layer. VTOT less than negative coercive voltage Vc‑ after polarization switching (e) assuming no leakage current through the DE layer and (f)

assuming the existence of leakage current through the DE layer. Type of

charges: black, ferroelectric polarization; blue, dielectric polarization;

red, interfacial trapped charge.

So, the C−V and P−E characteristics behave like a linear dielectric insulator. Second, if VFE,init > Vc but tDE is sufficiently thick, the FE layer cannot be fully polarized. As the polarization

switching happens, VDE increases until VFE reaches Vc, and the polarization process cannot continue. In this case, the total charge in the FE layer (QFE) can be approximated as ϵDE(VTOT −Vc)/tDE, where we have ferroelectric polarization charge (PFE) < Pr and VDE,final = QFE/(ϵDE/tDE). Note that PFE ≅ QFE = QDE if the PFE is significantly larger than the dielectric charge. Such an assumption is made for the simplicity of qualitative discussion and does not affect the conclusion. The numerical simulation including the difference of PFE and QFE gives the same conclusion. Third, if the DE layer is thin enough so that the

second criterion is not meet anymore, we can have the FE layer

fully polarized. So VDE can be estimated as VDE,final = Pr/(ϵDE/ tDE). It is clear that if QFE is larger than the maximum charge

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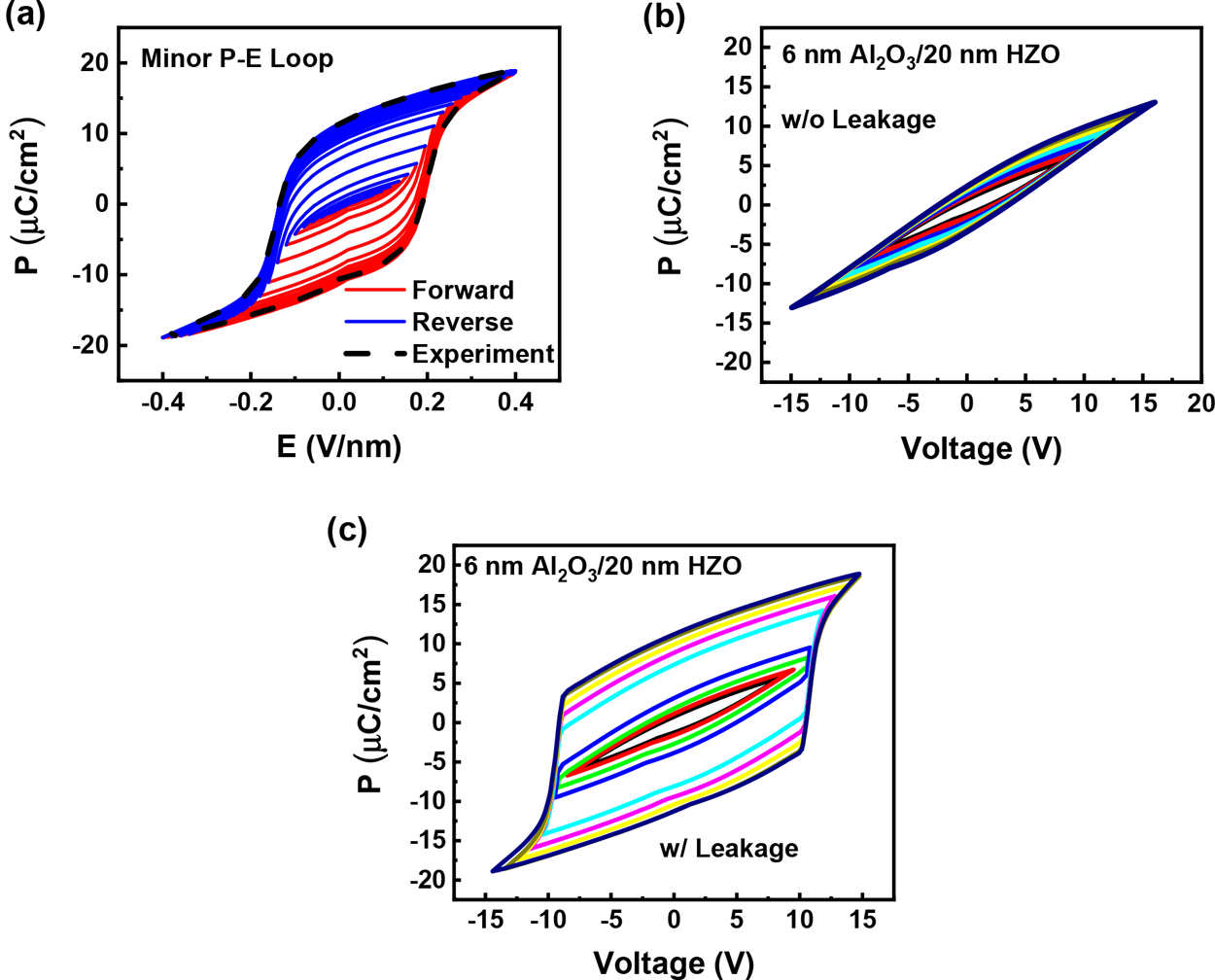


Figure 6. (a) Simulation of minor loops in an FE HZO capacitor. (b) Simulation without leakage current of P−V hysteresis loops in a 6 nm Al2O3/20 nm HZO capacitor at different voltage sweep ranges. (c) Simulation with leakage current of P−V hysteresis loops in a 6 nm Al2O3/20 nm HZO capacitor at different voltage sweep ranges.

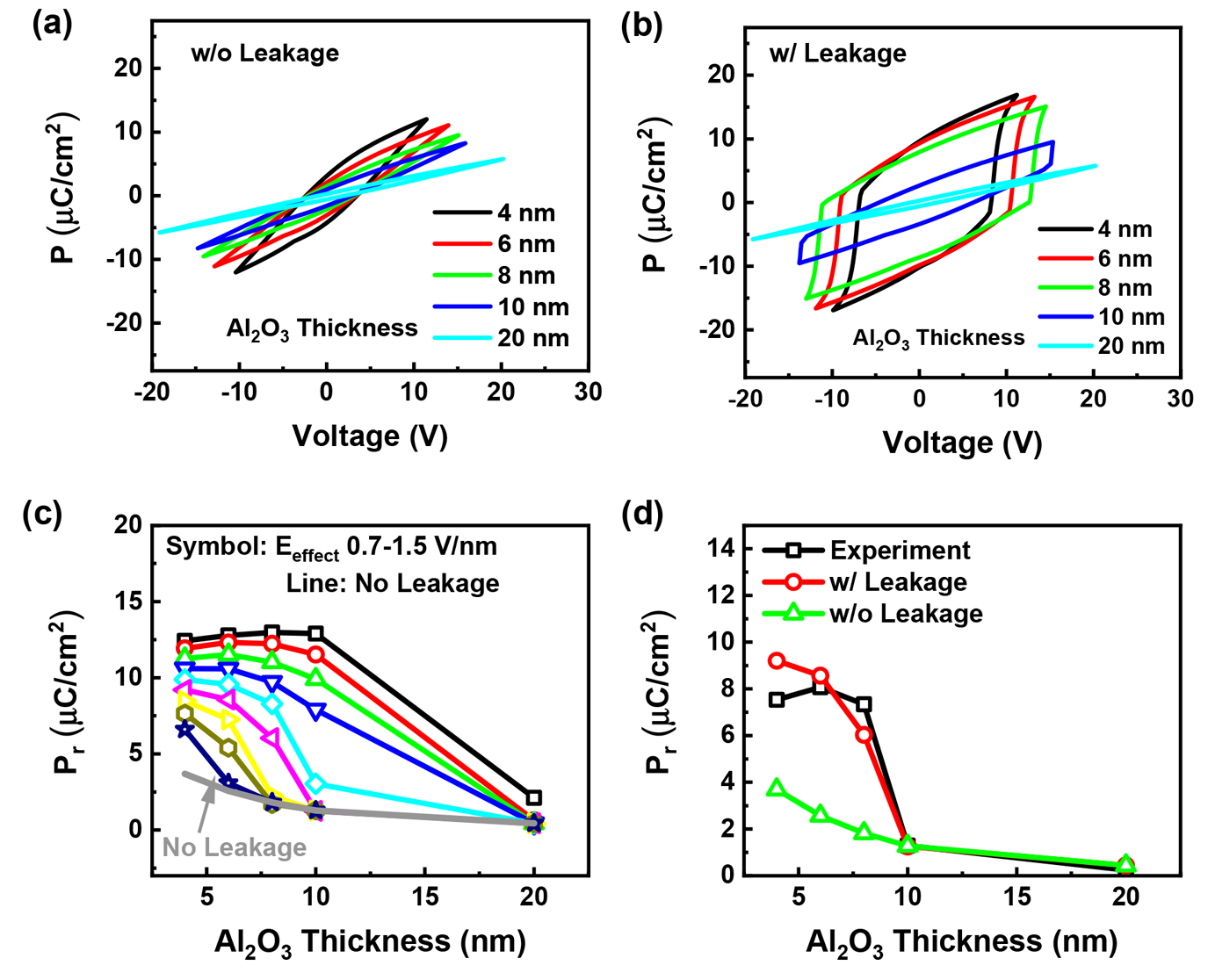


Figure 7. Simulation (a) without leakage current and (b) with leakage current of P−V hysteresis loops of FE/DE capacitors with 20 nm HZO and different Al2O3 thicknesses. (c) Remnant polarization versus Al2O3 thickness on both without leakage-current and with leakage-current assumptions at different Eeffect. (d) Comparison of experimental results on Pr vs Al2O3 thickness with simulation results, with and without leakage-assist switching.

P−E curve. If there is not enough charge from Qit and QDE, the FE layer always exhibits a minor loop with less Pr. Figure 6(b) shows the simulation of the P−V hysteresis loops in a 6 nm Al2O3/20 nm HZO capacitor at different voltage sweep ranges, assuming no leakage current. Figure 6(c) shows the simulation of the same structure but using the leakage-assist-switching model with leakage current from the DE layer. It is obvious that a

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studied experimentally. The leakage-assist-switching model can also simulate the thickness-dependent behavior. Figure 7(a) shows the simulation of the P−V hysteresis loop of the FE/DE stack with 20 nm HZO and different Al2O3 thicknesses, assuming no leakage current. Figure 7(b) shows the simulation of the same structure but using the leakage-assist-switching model. The specific voltage sweep ranges are selected according to the experimental results, as shown in Figure 4(b). Modeling and experiments are in great agreement. The model also successfully predicts the loss of Pr in the FE/DE stack with a thick DE layer because of the voltage division and no leakage current. Figure 7(c) shows the Pr versus thickness comparison in the without leakage model and with leakage model with different Eeffect, suggesting the FE/DE stack with a leakier DE layer can have a larger Pr. Figure 7(d) compares the experimental results on Pr vs Al2O3 thickness with simulation results, showing the leakage-assist-switching model matches well with experimental results in terms of thickness dependence. The above results provide new insights to understand the large amount of reported experimental results in NC-FETs usually with FE/DE stacks. FE and FE/DE are fundamentally different in terms of coercive field, Pr, switch speed, and many others.

The impact of internal metal is studied by comparing type C and type D capacitors (see [Supplementary Section 1](http://pubs.acs.org/doi/suppl/10.1021/acsaelm.9b00092/suppl_file/el9b00092_si_001.pdf)). The FE/ DE stacks with internal metal and without internal metal are physically very different. If the internal metal gate becomes the externally connected metal wires or the internal metal gate is physically connected to measurement equipment, the required balanced charges can be provided even externally. All these facts are extremely important to understand and interpret the experimental observation related to Fe-FETs and NC-FETs. The so-called interfacial coupling effect or capacitance enhance-ment was observed in previous reports.19,27−30This interfacial coupling effect can improve the equivalent oxide thickness of an FE/DE gate stack, which is also observed in the HZO/Al2O3 FE/DE stack as shown in [Supplementary Section 2](http://pubs.acs.org/doi/suppl/10.1021/acsaelm.9b00092/suppl_file/el9b00092_si_001.pdf). The above understanding of ferroelectric switching process helps to just apply ferroelectric polarization switching (sometimes calls transient negative capacitance effect) to explain the DC enhancement of ferroelectric-gated transistors without invoking the QSNC concept (see [Supplementary Section 3](http://pubs.acs.org/doi/suppl/10.1021/acsaelm.9b00092/suppl_file/el9b00092_si_001.pdf)). The operation speed of such transistors could be eventually limited by the ferroelectric switching speed,31which needs to be thoroughly investigated still.

■CONCLUSION   
In summary, the ferroelectric polarization switching in FE HZO in the HZO/Al2O3 FE/DE stack is investigated systematically by C−V and P−V measurements. The thickness of the dielectric layer is found to have determinant impact on the ferroelectric polarization switching of HZO. The suppression of ferroelec-tricity is observed with a thick linear dielectric layer. In the gate stacks with thin dielectric layers, a full polarization switching of the ferroelectric layer is found possible by the proposed leakage-current-assist mechanism through the ultrathin dielectric layer. The numerical simulation using the leakage-assist-switching model matches very well with the experimental results.

■ASSOCIATED CONTENT \* Supporting Information

The Supporting Information is available free of charge on the [ACS Publications website](http://pubs.acs.org) at DOI: [10.1021/acsaelm.9b00092](http://pubs.acs.org/doi/abs/10.1021/acsaelm.9b00092).

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